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Application No. 09/319,258

REMARKS/ARGUMENT**Summary of Status of Amendments and Office Action**

In the present amendment, claims 1, 2 and 9 are amended, and claims 50-54 are added. Therefore, claims 1-12, 22-27 and 44-54 are pending in the application with claims 1, 2, 6, 7, 9, 11 being independent claims.

Entry of this amendment after final rejection is appropriate because the amendment clarifies the claims in accordance with the Examiners' comments made during the interview that will be discussed below. Moreover, entry is appropriate because the finality of the Office Action is premature for the reasons that are discussed in the arguments below.

Support for the newly-added claims appears throughout Applicants' originally filed application including the original claims and the specification, for example, at page 9, beginning at line 6, and the last full paragraph on page 16.

Claims 6, 8, 11, 12, 27, 46, 47 and 49 are allowed.

Claims 1-5, 9, 10, 22-26, 44, 45 and 48 are rejected.

Claims 1-5, 22-26, 44 and 45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura, U.S. Patent No. 5,517,758.

Claims 1, 5, 25, 26 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, U.S. Patent No. 5,517,758.

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Claims 2, 24 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, U.S. Patent No. 5,517,758, in view of Adlam et al. (hereinafter "Adlam"), U.S. Patent No.5,861,076.

Claims 10 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, U.S. Patent No. 5,517,758.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, U.S. Patent No. 5,517,758, in view of Akahoshi et al. (hereinafter "Akahoshi"), U.S. Patent No 4,970,107.

Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, U.S. Patent No. 5,517,758, in view of Adlam, U.S. Patent No.5,861,076, and further in view of Akahoshi, U.S. Patent No 4,970,107.

Reconsideration and allowance of the application are respectfully requested.

Discussion Of January 28, 2004 Interview

Applicants express appreciation for the courtesies extended by Examiners John Vigushin and Jose H. Alcala at a personal interview with Applicants' representative Arnold Turk on January 28, 2004 at the Patent and Trademark Office.

During the interview, Applicants' invention and the prior art were thoroughly discussed along with proposed amendments to claims 1, 2 and 9 to even further clarify the terminology therein. In particular, the language of claims 1 and 2 was proposed to be amended to include plural terminology for the circuits. Moreover, amendment of claim 9 was proposed to modify the

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position of certain language, as included in the amendment herein, and possible deletion of language regarding plating.

With respect to the prior art, the Examiners clarified the rejections of record, and also presented further arguments making a prior art combination that is not actually set forth in the rejections of record. In particular, the Examiners recognize that Nakamura, U.S. Patent No. 5,517,758, does not explicitly disclose roughening of the conductor circuit, and, in fact, discloses roughening of the resin. However, the Examiners asserted that roughening of the conductor circuit is inherent in Nakamura. In this regard, they assert that when the conductor circuit of Nakamura is applied it will have an outer surface roughness due to its dipping into the roughness on the resin. The Examiners pointed to Fig. 1D to assert that this figure depicts a wavy surface on the conductor circuit. In response, arguments were presented that drawings in a patent are not to scale and there is no disclosure of a surface roughness. Moreover, it was argued that for inherency to be present, the result must be certain, not a mere chance. Arguments were presented that roughening of the resin surfaces is disclosed in Nakamura and not for the surface asserted to be roughened by the Examiners. However, the Examiners contended that the terminology "roughened layer" is broad.

The Examiners also made assertions regarding the disclosure of Akahoshi, U.S. Patent No. 4,970,107 in an attempt to establish obviousness of forming a roughened layer on a conductor circuit upper surface. In particular, the Examiners contended that Akahoshi discloses roughened surfaces on conductor surfaces, and that even if a roughened layer is not inherent, it would have been obvious to modify Nakamura with a roughened layer on the conductor circuit to have increased strength as taught by Akahoshi.

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Further, the Petition for change of inventorship filed December 3, 2002 was discussed. The Examiners were of the opinion that another area of the Office would handle the Petition. However, it was argued that such matters are handled by the Examiner, and required immediate handling because inventorship can be tied into prior art considerations. The Examiners agreed and after checking with another unit at the Patent and Trademark Office confirmed that this matter is handled by the Examiner. Therefore, it was agreed that the change of inventorship should be handled by the Examiner in the next communication from the Patent and Trademark Office.

Still further, arguments were presented that the finality of the Office Action was premature in view of new grounds of rejection based upon Akahoshi, U.S. Patent No. 4,970,107. The Examiners indicated that they would review the finality of the Office Action upon submission of a response.

Arguments as presented during the interview are included in the remarks herein.

Request For Withdrawal Of Finality Of Office Action

As discussed with the Examiners during the above-noted interview, Applicants respectfully submit that the finality of the Office Action is premature because the Office Action does not address all issues, and raises new issues that are not necessitated by Applicants' amendment.

First, Applicants respectfully submit that Applicants' Petition for Correction of Inventorship Under 37 C.F.R. 1.48(b), which was filed December 3, 2002, has not been acted upon in either the Office Action mailed April 23, 2003 or the present Final Office Action. Therefore, the

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action is not a complete action on the merits, does not address all issues, and therefore has been made final prematurely.

Moreover, the present Final Office Action cites for the first time, Akahoshi, U.S. Patent No. 4,970,107, and utilizes this newly-cited document in two separate rejections, i.e., the obviousness rejection of claims 3 and 4 over Nakamura in view of Akahoshi, and the obviousness rejections of claims 22 and 23 of Nakamura in view of Adlam, and further in view of Akahoshi. Applicants respectfully submit that their clarifying amendment of claims 1 and 2 did not necessitate new grounds of rejection of claims 3, 4, 22 or 23 including Akahoshi. In this regard, as pointed out by Applicants in their previous response, the claims were amended therein to include what should be considered to be cosmetic changes to utilize language that is preferred by the Examiner. As stated therein, this language was not intended to change the claim scope, with the claims merely being amended to advance the application to issue.

Applicants respectfully submit that they should be afforded an opportunity to address new grounds of rejection in a non-final Office Action, and to have a non-final Office Action that addresses all outstanding issues. According, withdrawal of finality of the Office Action is respectfully requested accompanied by entry of the present amendment.

Response to 35 U.S.C. 112, Second Paragraph, Rejection

Claims 1-5, 22-26, 44 and 45 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

In response, and as noted above, the claims are amended herein to include the amendments

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to claims 1 and 2 discussed with the Examiners during the above-noted interview.

Moreover, claim 9 is partially amended herein as discussed with the Examiners during the above-noted interview regarding the placement of certain language in the claims. However, plating language has been retained in the claim. In particular, claim 9 includes therein, "a roughened layer on at least a part of the surface of the under layer conductor circuit connected to the viahole, said roughened layer having a roughened surface formed by etching treatment, polishing treatment, redox treatment or plating treatment".

Moreover, Applicants note that the Examiner has included in his remarks an indication as to how claim 9 is being construed by the Examiner. However, this is in contrast to the indication in Applicants' previous response wherein it was indicated that the claim recitation clearly indicates that the roughened layer is on at least a part of the surface of the under layer conductor circuit connected to the viahole. It was pointed out that the surface of the viahole need not be roughened in this embodiment, but can be roughened. Moreover, it was pointed out that the roughened layer on the under layer conductor circuit can be formed on, not only the portion connecting to the viahole, but also the whole surface of the under layer conductor circuit, such as disclosed in the specification at page 11, second paragraph.

In view of the above amendments which should be considered to be cosmetic, Applicants respectfully submit that the indefiniteness rejection should be withdrawn.

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Request For Granting Of Petition For Correction of Inventorship

As discussed with the Examiners during the above-noted interview, a Petition for Correction of Inventorship Under 37 C.F.R. 1.48(b) has been filed on December 3, 2002, but has not been addressed in the previous Office Action or in this Final Office Action. Accordingly, it is once again respectfully requested that the next communication from the Patent and Trademark Office acknowledge the Petition, and indicate that it has been granted whereby the inventorship of the presently claimed invention has been corrected.

Response To Rejections Based Upon Prior Art

As noted above, the following rejections are present in the Office Action

Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura, U.S. Patent No. 5,517,758.

Claims 1, 5, 25, 26 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, U.S. Patent No. 5,517,758.

Claims 2, 24 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, U.S. Patent No. 5,517,758, in view of Adam, U.S. Patent No. 5,861,076.

Claims 10 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, U.S. Patent No. 5,517,758.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, U.S. Patent No. 5,517,758, in view of Akahoshi, U.S. Patent No. 4,970,107.

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Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, U.S. Patent No. 5,517,758, in view of Adlam, and further in view of Akahoshi.

With regard to the rejection of independent claim 9, Applicants note that independent claim 9 is directed to a multilayer printed circuit board comprising a substrate provided with an under layer conductor circuit, an interlaminar insulating layer formed thereon and an upper layer conductor circuit formed on the interlaminar insulating layer, and a viahole connecting both the conductor circuits to each other, in which the viahole is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer on at least a part of the surface of the under layer conductor circuit connected to the viahole, said roughened layer having a roughened surface formed by etching treatment, polishing treatment, redox treatment or plating treatment.

Thus, amongst other features recited in Applicants' claim 9, the claim includes that the viahole is comprised of an electroless plated film and an electrolytic plated film, and includes a roughened layer on at least a part of the surface of the under layer conductor circuit connected to the viahole, said roughened layer having a roughened surface formed by etching treatment, polishing treatment, redox treatment or plating treatment.

In contrast to Applicants' disclosed and claimed invention, Applicants again point out that Nakamura does not disclose a roughened layer on at least a part of the surface of the conductor surface, as recited in Applicants' claims. Instead, Nakamura discloses that the insulating resin layer, such as insulating resin layer 74, and the viaholes 75 and the through-holes 76 are roughened. This is similar to the roughened surfaces discussed in the Background Art section of Applicants' specification. Moreover, Nakamura does not disclose that the under layer 73 is produced from an

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electroless plated film and an electrolytic plated film. The rejection tries to overcome this deficiency by referring to Nakamura at column 9, lines 59-67 and column 10, lines 1-3. However, this disclosure does not overcome the above-noted deficiencies.

In particular, in this portion of Nakamura, it is disclosed that a first circuit conductor layer 93 is formed on each surface of an insulating substrate 91. Then, resistor film 100 is disclosed to be formed on at least one of the surfaces of the insulating substrate 91 to form a resistance-forming substrate (the core substrate) as shown in FIG. 9A. The resistor film 100 is disclosed to be formed as follows: the insulating substrate 91 is coated with a carbon resin resistor paste by the screen printing, and hardened with heat. Then, the shape of the resistor film 100 is adjusted by laser trimming and the resistance value of the resistor film 100 is adjusted. Alternatively, metal resistor film can be formed as the resistor film 100 by the electroless plating method.

Next, Nakamura discloses that the same procedures as shown in FIGS. 7A to 7F are performed, using the core substrate shown in FIG. 9A. More specifically, Nakamura discloses an insulating resin layer 94 is coated on each surface of the core substrate, and then via holes 95 and through-holes 96 are formed in the core substrate. Then, the surface of the insulating resin layer 94 and the inner walls of the via hole 95 and the through-hole 96 are disclosed to be appropriately roughened by the dry sandblasting treatment and the chemical etching using a potassium permanganate solution. Then, a conductive metal layer is disclosed to be formed on the entire surface of the substrate by the electroless copper plating and the electrolytic copper plating. It is then disclosed that a second circuit conductor layer 98 is then formed by a known technique such

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as the photoetching, and the resulting multi-layered printed wiring board having the substrate as shown in FIG. 9B is disclosed to be fabricated.

As can be seen from the above, this portion of Nakamura does not teach or suggest, amongst the other features recited in claim 9, a viahole comprised of an electroless plated film and an electrolytic plated film, and a roughened layer on at least a part of the surface of the under layer conductor circuit connected to the viahole, said roughened layer having a roughened surface formed by etching treatment, polishing treatment, redox treatment or plating treatment.

During the above-noted interview, the Examiners asserted that a roughened surface would be inherent from the disclosure of Nakamura, and specifically pointed to Fig. 1D for a showing of a wavy surface. However, such a surface is not a roughened surface to one having ordinary skill in the art, and this is, especially apparent from the fact that Nakamura specifically discloses treating the insulating layer to form a roughened surface. In any event, claim 9 explicitly recites that the roughened layer has a roughened surface formed by etching treatment, polishing treatment, redox treatment or plating treatment, and the structure achieved by such roughening treatment would not be the same as disclosed in Nakamura.

Still further, drawings in a patent are not to scale, and disclosure cannot be read into the drawings unless it is consistent with the specification. In the instant situation, the disclosure teaches roughening another surface, and does not teach or suggest a roughened layer on at least a part of the surface of the under layer conductor circuit connected to the viahole, the roughened layer having a roughened surface formed by etching treatment, polishing treatment, redox treatment or plating treatment. The rejection cannot merely disregard structure associated with

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limitations recited in the claim.

Moreover, the Examiner is reminded that in order for inherency to be present the Examiner has the burden of showing that the result indicated by the Examiner is the necessary result, and not merely a possible result. In re Oelrich, 212 U.S.P.Q. 323 (CCPA 1981); Ex parte Keith et al., 154 U.S.P.Q. 320 (POBA 1966). The fact that a prior art article may inherently have the characteristics of the claimed product is not sufficient. Ex parte Skinner, 2 U.S.P.Q.2d 1788 (BPAI 1986).

As the Board of Patent Appeals and Interferences states in Ex parte Levy, 17 U.S.P.Q.2d 1461, 1463;

However, the initial burden of establishing a prima facie basis to deny patentability to a claimed invention rests upon the examiner. In re Piasecki, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984). In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); In re Oelrich, 666 F.2d 578, 212 USPQ 323 (CCPA 1981); In re Wilding, 535 F.2d 631, 190 USPQ 59 (CCPA 1976); Hansgirk v. Kemmer, 102 F.2d 212, 40 USPQ 665 (CCPA 1939). in order for inherency to be present it must be a necessary result, and not merely a possible results. Ex parte Keith and Turnquest, 154 U.S.P.Q. 320 (B.O.A. 1966).

In the instant situation, the Examiner has not provided any evidence to support the position that, amongst other features in Applicants' claim 9, Nakamura would by necessity include a viahole comprised of an electroless plated film and an electrolytic plated film, and a roughened layer having a roughened surface formed by etching treatment, polishing treatment, redox treatment or plating treatment.

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Regarding independent claims 1 and 2, Applicants note that independent claim 1 is directed to a multilayer printed circuit board comprising a plurality of interlaminar insulating layers and conductor circuits, said printed circuit board being formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and forming at least a second conductor circuit and a second interlaminar insulating layer on the first interlaminar insulating layer, wherein the conductor circuits are comprised of an electroless plated film and an electrolytic plated film, and a roughened layer formed by a roughening treatment on at least a part of the surface of the conductor circuits.

Moreover, Applicants' independent claim 2 is directed to a multilayer printed circuit board comprising a plurality of interlaminar insulating layers and conductor circuits, said printed circuit board being formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and forming at least a second conductor circuit and a second interlaminar insulating layer on the first interlaminar insulating layer, wherein the conductor circuits are comprised of an electroless plated film and an electrolytic plated film, and a roughened layer formed by a roughening treatment on at least a part of the surface of the conductor circuits, and the surface of the roughened layer is covered with a layer of a metal having an ionization tendency of more than copper but not higher than titanium, or of a noble metal.

Accordingly, for the reasons discussed above, it is apparent that Nakamura does not teach or suggest the invention recited in Applicants' independent claims 1 and 2, which include, amongst other features, that the conductor circuits are comprised of an electroless plated film and an electrolytic plated film, and a roughened layer formed by a roughening treatment on at least a part

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of the surface of the conductor circuits. For the reasons discussed above, Nakamura does not teach or suggest conductor circuits comprises of an electroless plated film and an electrolytic plated film, and a roughened layer formed by a roughening treatment on at least a part of the surface of the conductor circuits. Nakamura discloses roughening an insulating resin, and does not teach or suggest the structure recited in Applicants' claims.

In the rejection of independent claim 1, the rejection relies upon the disclosure of Nakamura at column 9, lines 25-27 and Fig. 1D. However, this disclosure does not teach or suggest Applicants' invention for similar reasons as noted with respect to claim 9. Nakamura does not inherently disclose conductor circuits comprised of an electroless plated film and an electrolytic plated film, and a roughened layer formed by a roughening treatment on at least a part of the surface of the conductor circuits.

With respect to claim 2, Applicants note that the rejection relies upon Nakamura in view of Adlam. However, Adlam does not overcome the deficiencies of Nakamura. Accordingly, whether or not it would have been obvious to make the asserted combination, which Applicants submit is not proper, the presently claimed invention would not be present.

Regarding the rejection of claims 25 and 26, Applicants note that these claims depend upon claims 3 and 4, respectively. Moreover, claims 3 and 4 are rejected based upon Nakamura in view of Akahoshi. Therefore, it is clear that the rejection of claims 25 and 26 is inappropriate, because it does not include Akahoshi in the rejection. Therefore, if the rejection of claims 25 and 26 is maintained, the rejection should be clarified.

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Regarding the assertion of obviousness based upon mere duplication of parts, Applicants respectfully submit that this is not the situation here. The claims are directed to a multilayer printed circuit board, and the multiple layers contribute to its structure and function.

Regarding the rejection of claims 5, 10, 24, 25, 26 and 48, the rejection asserts that the features of these claims would have been obvious. However, the rejection merely makes a naked assertion, and does not utilize any supporting documentary evidence to establish obviousness of having a roughened layer which is a plated layer of copper-nickel-phosphorus alloy. If this ground of rejection is maintained, the Examiner is respectfully requested to provide documentary evidence to establish that it would have been obvious to have a roughened layer which is a plated layer of copper-nickel-phosphorus alloy in combination with the other elements of Applicants' claims.

Regarding claims 44, 45 and 48, the Examiner is respectfully requested to provide support for the assertion that Nakamura inherently teaches that the electrolytic plated film is formed on the electroless plated film. The rejection merely refers to disclosure in Nakamura, but does not indicate how this disclosure inherently teaches Applicants' invention. As noted above, the rejection must establish that the asserted structure is necessarily present in the cited document.

Regarding claims 3, 4, 22 and 23, Applicants respectfully submit that Akahoshi does not overcome the deficiencies of either of Nakamura and/or Adlam. While Akahoshi discloses roughened surfaces on conductor surfaces, Akahoshi fails to teach or suggest two-layer structure of the conductor circuit in combination with a roughened surface formed thereon. In other words, Akahoshi fails to teach or suggest conductor circuits each comprised of an electroless layer on at least a part of the surface of each conductor circuit. With such a combined structure, since the

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electrolytic plated film is softer and more malleable than the electroless plated film, the conductor circuit is able to follow size change of the interlaminar insulating resin layer as an upper layer even if warping of the board is generated in the heat cycle, as disclosed in the second paragraph of page 9 of Applicants' specification.

Akahoshi also fails to teach or suggest a two-layered structure of a viahole comprised of an electroless plated film and an electrolytic plated film, and including a roughened layer on at least a part of the surface of the under layer conductor circuit connected to the viahole, said roughened layer having a roughened surface formed by etching treatment, polishing treatment, redox treatment or plating treatment.

With such combined structure, since the electrolytic plated film is softer and more malleable than the electroless plated film, the viahole is able to follow size change of the interlaminar insulating resin layer as an upper layer even if warping of the board is generated in the heat cycle. Moreover, the viahole is constructed at the inner layer side with the hard electroless plated film and also such an electroless plated film is adhered to the under layer conductor circuit through the roughened layer, so that the viahole is not peeled off from the under layer conductor circuit in the heat cycle. Because the metal layer encroached by the roughened layer is the harder electroless plated film, and hence breakage at the metal layer is rarely caused even when peeling force is applied, as disclosed in the first full paragraph of page 10 of Applicants' specification.

In short, when the viahole is comprised of only the electrolytic plated film, even if it is adhered to the under layer conductor circuit through the roughened layer, the electrolytic plated film itself is soft and is apt to peel off due to the heat cycle. While, when the viahole is comprised

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of only the electroless plated film, it can not follow size change of the interlaminar insulating resin layer and hence cracking is caused in the interlaminar insulating resin layer on the viahole. In the printed circuit board according to the present invention, the viahole is comprised of the electrolytic plated film and the electroless plated film and connected to the under layer conductor circuit through the roughened layer, so that the occurrence of cracks generated in the interlaminar insulating resin layer on the viahole, and peeling between the viahole and the under layer conductor circuit in the heat cycle can be prevented at the same time, as can be seen from Applicants' specification at page 10, large full paragraph.

Accordingly, Akahoshi does not overcome any of the deficiencies of Nakamura and/or Adlam.

... Thus, Applicants once again respectfully submit that the only teaching or suggestion that would lead one having ordinary skill in the art to arrive at Applicants' invention is within Applicants' disclosure, and the use of such disclosure by the Examiner is improper. In order to support the conclusion that the claimed invention is either anticipated or rendered obvious over the prior art, the prior art must either expressly or inherently teach the claimed invention or the Examiner must present a convincing line of reasoning why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references. Ex parte Clapp, 227 USPQ 972 (B.O.A. 1985).

In view of the above, the rejections of record should be withdrawn.

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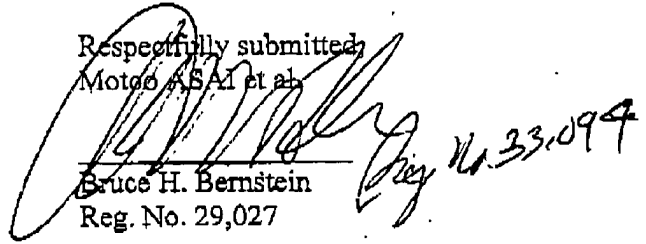
CONCLUSION

For the reasons advanced above, Applicants respectfully submit that all pending claims patentably define Applicants' invention.

Allowance of the application with an early mailing date of the Notices of Allowance and Allowability is therefore respectfully requested.

Should the Examiner have any further comments or questions, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
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